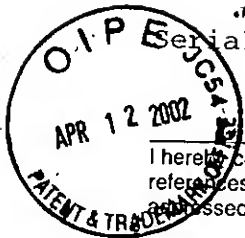


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Serial No. 10/015,921

Technology Center 2100

IBM Docket No. RPS920010132US

PATENT

#4

I hereby certify that this correspondence (37 CFR 1.97(b)) and attached documents (i.e., PTO 1449 and copies of all cited references) are being deposited with the United States Postal Service as first class mail in an envelope with sufficient postage addressed to: Assistant Commissioner for Patents, Washington, DC 20231.

*Karen Orzechowski*  
Karen Orzechowski

APRIL 9, 2002  
Date of Deposit

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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

In re application of  
R. T. Bailis, et al.

Serial No. 10/015,921

Filed: Dec. 10, 2001

: April 8, 2002  
: IBM Corporation - 9CCA/B002  
: P.O. Box 12195  
: Research Triangle Park,  
: North Carolina 27709  
: Unit: 2811

For: METHOD AND SYSTEM FOR USE OF A FIELD PROGRAMMABLE GATE ARRAY (FPGA) CELL  
FOR CONTROLLING ACCESS TO ON-CHIP FUNCTIONS OF A SYSTEM ON A CHIP (SOC)  
INTEGRATED CIRCUIT

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT  
WITHIN THREE MONTHS OF FILING OR BEFORE MAILING  
OF FIRST OFFICE ACTION (37 CFR 1.97(b))

Assistant Commissioner for Patents  
Washington, DC 20231  
Sir:

The information disclosure statement transmitted herewith is being filed within three months of the filing date of the application or date of entry into the national stage of an international application or before the mailing date of a first Office action on the merits, whichever occurs last, under 37 CFR 1.97(b); no fee is required.

This Information Disclosure Statement is being submitted in connection with the above-identified application for patent. Applicants submit herewith patents, publications or other information of which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 C.F.R. § 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 C.F.R. § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information

Serial No. 10/015,921

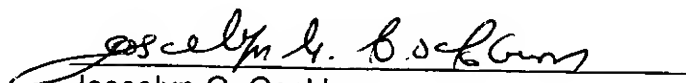
**PATENT**  
*IBM Docket No. RPS920010132US1*

as defined in 37 C.F.R. § 1.56(a) exists.

The attached form, PTO-1449, provides a listing of patents, publications, or other information as required by 37 C.F.R. § 1.98(a)(1).

A copy of each of the items identified on the attached Form PTO-1449 is supplied herewith.

Respectfully submitted,

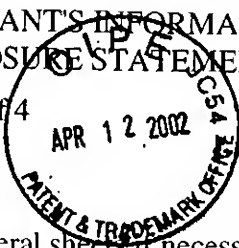
  
Joscelyn G. Cockburn  
Reg. No. 27,069  
Attorney of Record

JGC:ko  
919-543-9036  
FAX 919-254-2649

FORM PTO-1449 (Modified)

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## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	6 1 3 4 1 7 3	Oct. 17, 2000	Cliff, et al.	265	230.03	Nov. 2, 1998
	6 1 7 3 4 1 9B1	Jan. 9, 2001	Barnett	714	28	May 14, 1998
	6 1 7 8 5 4 1B1	Jan. 23, 2001	Joly, et al.	716	17	Mar. 30, 1998
	6 1 8 1 1 5 9B1	Jan. 20, 2001	Rangasayee	326	39	Aug. 25, 1998
	6 1 8 2 2 0 6B1	Jan. 30, 2001	Baxter	712	43	Feb. 26, 1998
	6 1 8 2 2 4 7B1	Jan. 30, 2001	Hermann, et al.	714	39	Oct. 27, 1997

## FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
					YES	NO

## OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

BB	C. E. Kuhlmann et al., U.S. Pending Patent Application Serial No. 10/016346 (docket RPS920010125US1), "Field Programmable Network Processor and Method for Customizing a Network Processor"
CC	R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/016772 (docket RPS920010126US1), "Method and System for Use of an Embedded Field Programmable Gate Array Interconnect for Flexible I/O Connectivity"

EXAMINER

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## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	6 1 9 1 6 1 4B1	Feb. 20, 2001	Schultz, et al.	326	41	Aug. 13, 1999
	6 2 0 9 1 1 8B1	Mar. 27, 2001	LaBerge	716	1	Jan. 21, 1998
	6 2 1 1 6 9 7B1	Apr. 3, 2001	Lien, et al.	326	41	May 25, 1999
	6 2 1 9 8 1 9B1	Apr. 17, 2001	Vashi, et al.	716	3	Jun. 26, 1998
	6 2 1 9 8 3 3B1	Apr. 17, 2001	Solomon, et al.	717	5	Dec. 11, 1998
	6 2 2 3 1 4 8	Apr. 24, 2001	Stewart, et al.	703	25	Aug. 14, 1998

## FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation
					YES NO

## OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

DD	R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/016449 (docket RPS920010127US1), "Method and System for Use of a Field Programmable Gate Array Function within an Application Specific Integrated Circuit (ASIC) to Enable Creation of a Debugger Client within the ASIC"
EE	R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/016448 (docket RPS920010128US1), "Method and System for Use of a Field Programmable Function within an Application Specific Integrated Circuit (ASIC) to Access Internal Signals for External Observation and Control"

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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	6 2 2 3 3 1 3B1	Apr. 24, 2001	How, et al.	714	724	Dec. 5, 1997
	6 2 2 6 7 7 6B1	May 1, 2001	Panchul, et al.	716	3	Sep. 16, 1997
	6 2 3 0 1 1 9B1	May 8, 2001	Mitchell	703	27	Feb. 6, 1998
	6 2 3 7 0 2 1B1	May 22, 2001	Drummond	709	201	Sep 25, 1998
	6 2 4 7 1 4 7B1	Jun. 12, 2001	Beenstra, et al.	714	39	Jun. 12, 2001
	6 2 4 9 1 4 3B1	Jun. 19, 2001	Zaveri, et al.	326	40	Jan. 15, 1998

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation
					YES NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

FF	R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/015922 (docket RPS920010129US1), "Method and System for Use of a Field Programmable Interconnect within an ASIC for Configuring the ASIC"
GG	R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/015920 (docket RPS920010130US1), "Method and System for Use of a Field Programmable Function within a Chip to Enable Configurable I/O Signal Timing Characteristics"

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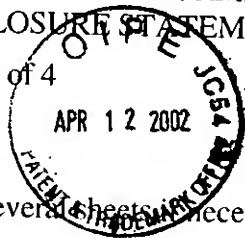
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EXAMINER INITIALS	DOCUMENT NUMBER							DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	6	2	5	2	4	2	2B1	Jun. 26, 2001	Patel, et al.	326	80	Sep. 22, 1999
	6	2	5	3	2	6	7B1	Jun. 26, 2001	Kim, et al.	710	103	Jul. 31, 1998
	6	2	5	6	2	9	6B1	Jul. 3, 2001	Ruziak, et al.	370	277	Dec. 17, 1997
	6	2	6	0	0	8	7B1	Jul. 10, 2001	Chang	710	100	Mar. 3, 1999
	6	2	6	0	1	8	2B1	Jul. 10, 2001	Mohan, et al.	716	12	Mar. 27, 1998
	6	2	6	0	1	8	5B1	Jul. 10, 2001	Sasaki, et al.	716	18	Apr. 24, 1996

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUBCLASS	Translation	
												YES	NO

## OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

HH		R. T. Bailis et al., U.S. Pending Patent Application Serial No. 10/015923 (docket RPS920010131US1). "Method and System for Use of a Field Programmable Function within a Standard Cell Chip for Repair of Logic Circuits"

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